IN THE CLAIMS:

1-7 (Cancelled)

8. (Currently amended) A method of forming a MOSFET having a recessed channel, comprising:

forming a [recessed] trench in a semiconductor substrate;

forming a gate ~~oxide~~ dielectric layer on an inner wall and a bottom of said [recessed] trench;

sequentially forming a gate conductive layer and a capping layer on the gate ~~oxide~~ dielectric layer so as to ~~completely~~ fill the [recessed] trench;

forming a gate electrode [that is overlapped by the gate conductive layer] having a first portion [filling the recessed trench by patterning the capping layer and the gate conductive layer] which rises over the semiconductor substrate and a second portion filling the trench by patterning the capping layer and the gate conductive layer, wherein the first portion [to] has[ve] a smaller critical dimension than that of the second portion [recessed trench]; and

forming a source/drain region by implanting impurity ions into the semiconductor substrate on both sides of the gate electrode.

9. (Currently amended) The method of claim 8, wherein forming the [recessed] trench comprises:

forming a rectangular trench in the semiconductor substrate using an [reactive ion beam] etch process; and

making the [recessed] trench have a round profile by further etching the trench using a chemical dry etch process.

10. (Original) The method of claim 9, wherein the rectangular trench is formed to a depth of about 1000Å to 1500Å and is further etched by about 100Å to about 200Å using a chemical dry etch process.

11. (Currently amended) The method of claim 8, wherein the gate ~~oxide~~ dielectric

layer is formed of one from the group consisting of: a silicon oxide layer, a titanium oxide layer, and a tantalum oxide layer.

12. (Currently amended) The method of claim 8, wherein the gate conductive layer comprises a conductive polysilicon layer that ~~completely~~ fills the [recessed] trench and a metal layer formed on the conductive polysilicon layer.

13. (Currently amended) The method of claim 8, wherein forming the [recessed] trench further compromises:

forming a sacrificial oxide layer by thermally oxidizing the semiconductor substrate; and

removing the sacrificial oxide layer using a wet etch process.

14. (Currently amended) The method of claim 8, wherein forming the gate electrode comprises recessing the gate conductive layer that fills the [recessed] trench to a depth of 500Å or less from the surface of the semiconductor substrate by adjusting the etching time.

15. (Original) The method of claim 8, further comprising forming spacers on the sidewalls of the gate electrode.

16. (Cancelled)

17. (New) The method of claim 14, further comprising forming spacers on the sidewalls of the gate electrode, wherein a portion of the spacers are extended into the semiconductor substrate.

18. (New) The method of claim 9, wherein the etch process is a reactive ion beam etch process.

19. (New) The method of claim 8, wherein the source/drain region is shallower than the bottom of the trench.

20. (New) A method of forming a MOSFET having a recessed channel, comprising:

forming a trench in a semiconductor substrate using a etch process;

forming a gate ~~oxide~~ dielectric layer on an inner wall and a bottom of said trench;

sequentially forming a gate conductive layer and a capping layer on the gate ~~oxide~~ dielectric layer so as to ~~completely~~ fill the trench;

forming a gate electrode having a first portion which rises over the semiconductor substrate and a second portion filling the trench by patterning the capping layer and the gate conductive layer, wherein the first portion has a smaller critical dimension than that of the second portion;

forming spacers on the sidewalls of the gate electrode, wherein a portion of the spacers are extended into the semiconductor substrate; and

forming a source/drain region by implanting impurity ions into the semiconductor substrate on both sides of the gate electrode,

and wherein forming the gate electrode comprises recessing the gate conductive layer that fills the trench to a depth of 500Å or less from a top surface of the semiconductor substrate by adjusting etching time.

21. (New) The method of claim 20, wherein the trench is formed to a depth of about 1000Å to about 1500Å and is further etched by about 100Å to about 200Å using a chemical dry etch process.

22. (New) The method of claim 20, wherein the source/drain region is shallower than the bottom of the trench.